5505

OTIS SPECIFICATION

1 INTRODUCTION

OTIS is a VLSI device designed in a 2 micron double metal CMOS process. The device is the next generation of audio technology from Ensoniq. This new chip achieves a new level of audio fidelity performance. These improvements are achieved through the use of frequency interpolation and on board real time digital filters. All calculations in the device are made with at least 16 bit accuracy. The major features of OTIS are:

48 PIN DUAL IN LINE PACKAGE

ON CHIP REAL TIME DIGITAL FILTERS

FREQUENCY INTERPOLATION

32 INDEPENDENT VOICES, UP FROM 25 IN DOCII

LOOP START AND STOP POSITIONS FOR EACH VOICE

BIDIRECTIONAL AND REVERSE LOOPING

68000 COMPATIBILITY FOR ASYNCHRONOUS BUS COMMUNICATION

ON BOARD PULSE WIDTH MODULATED D TO A

4 CHANNEL STEREO SERIAL COMMUNICATION PORT

INTERNAL VOLUME MULTIPLICATION AND STEREO PANNING

A TO D INPUT FOR POTS AND WHEELS

UP TO 10 MHz OPERATION

THEORY OF OPERATION

OTIS operates in a separate memory space called sound memory. The sound memory space can be up to 2 Mword of 16 bit ram. OTIS communicates to the microprocessor through its 16 bit data bus and 4 bit address bus. OTIS contains 32 independent voices each of which are controlled by 16 voice specific registers and 3 global registers. OTIS creates sound for each voice in succession by performing the following algorithm. The 20 bit integer portion of the 29 bit accumulator is placed on the Address Bus (A0 thru A19) along with a 1 bit bank select (BS) to select between 1Mword memory banks.

OTIS PINOUT

A17/D13 -	1	48	- VSS
A18/D14 -	2	47	- A16/D12
A19/D15 -	3	46	- A15/D11
BS -	4	45	- A14/D10
PWZERO -	5	44	- A13/D9
SER0 -	6	43	- A12/D8
SER1 -	7	42	- A11/D7
SER2 -	8	41	- A10/D6
SER3 -	9	40	- A9/D5
SERWCLK -	10	39	- A8/D4
SERLR -	11	38	- A7/D3
SERBCLK -	12	37	- A6/D2
RLO -	13	36	- A5/D1
RHI -	14	35	- A4/D0
LLO -	15	34	- CLKIN
LHI -	16	33	- CAS
POT -	17	32	- AMUX
DTACK -	18	31	- RAS
R/W -	19	30	- E
MS -	20	29	- IRQ
CS -	21	28	- A3
RES -	22	27	- A2
VSS -	23	26	- A1
VDD -	24	25	- A0

The sample data S1 is received from the Data Bus and placed in a temporary holding register. The accumulator is then incremented by one and placed on the Address Bus. This sample, S2, is used with the previous sample, S1, to compute SF, the actual sample.

The value SF is now transferred to the filter computation section. In this section a real time 4 pole digital filter is implemented as 4 one pole filters cascaded in a chain. The first two poles are fixed as low pass filters the second two poles can be set independently as either high pass or low pass.

The address generation for each voice consists of a 29 bit Voice Accumulator, a Loop Start Register, a Loop End Register, and a Control Register. The Voice Accumulator contains a 20 bit integer portion and a 9 bit fractional portion. The integer portion of the Voice Accumulator is used to address the external sound ram while the fractional portion is used in the interpolation calculation. The Control Register is used to control interrupts, the various modes of looping, stopping and starting the voice, and a 1 bit bank select to select a 1Mword bank of memory.

The three global registers are used to set the total number of active voices, the Voice Interrupt Vector, and the Page Register. There are nine additional registers for setting OTIS modes and testing the channel registers.

2 REGISTER DESCRIPTION

2.1 THE GLOBAL REGISTERS

The following section describes in detail the structure and purpose of each of the registers in the OTIS chip.

Page Register - F

The page register is used to access the set of 16 registers which control all aspects of a voice. The Page register appears at location F_{hex} in all pages. There are a total of 128 pages which can be accessed through the page register. Locations 0 thru A_{hex} of pages 0 to 31 control the most often used settings for each voice. Locations 1 thru 6 of pages 32 to 63 offer access to the temporary registers for the intermediate data used in the real time filter calculations. Locations 0 thru 8 of pages 64 to 127 access the serial communication registers and the special mode register.

Voice Interrupt Vector Register - IRQV - E

The Voice Interrupt Vector register is used by the microprocessor to determine which voice has caused an interrupt to occur. When a voice has its interrupt enabled in its corresponding control register and the proper events occur to cause an interrupt to be issued, the voice number is placed into this register so that the processor can read the value and determine which voice requires servicing. The IRQ output line of the OTIS chip will go high after the processor reads this register. Bit 7 of this register is a monitor of the IRQ output line and bits 4 through 0 determine the voice interrupt. Conditions sufficient to cause an interrupt will be defined in the Interrupt Control Section.

Active Voice Register - ACT - D

The Active Voice Register defines how many voices are actually enabled to produce sound. This register uses bits 4 through 0, encoding values 31 through 0. The actual number of active voices is equal to the number in this register plus one. The number of active voices determines the output sample rate of OTIS. Each voice takes 1.6 microseconds to be processed if OTIS is running at 10MHz. When all 32 voices are active, this corresponds to a 19.5KHz sample rate. If only 16 voices are active, the sample rate is 39KHz.

2.2 THE VOICE SPECIFIC REGISTERS

The following section describes the registers which control a voice in OTIS. The registers for a specific voice are accessed using the A3-A0 address lines. The page register is used to direct the data flow to a particular voice. All bits in all the voice specific registers can be written to and read from. Note the abbreviation in parentheses following the register name may be used interchangeably.

The Control Register (CR) - 0

The Control Register is an eight bit register which directs various aspects of OTIS. The following is a list of control register bits and their function.

LP4,LP3 — The Filter Configuration bits define the four possible modes of the digital filter. The two bits used are referred to as LP4 and LP3, which are lowpass pole 4 and lowpass pole 3, respectively. The following chart indicates these configurations.

Filter Configuration and Coefficient Assignments

LP4	LP3	Filter Pole 4 Coefficient	Filter Pole 3 Coefficient
0	0	HP / K2	HP / K2
0	1	HP / K2	LP / K1
1	0	LP / K2	LP / K2
1	1	LP / K2	LP / K1

Note that the above chart shows both the mode of the filter pole as well as the coefficient value used in the filter computation. In the digital filter poles one and two are low pass and use coefficient K1.

CA1,CA0 — The Channel Assign information is a 2 bit code normally used to specify an output channel for the current voice. There are four serial output channels 0 to 3. Channel 0 is also connected to the pulse width modulated playback outputs.

IRQ — A status flag showing that this voice has requested service through the Voice Interrupt Vector or has an interrupt request pending and is waiting for the Voice Interrupt Vector to be cleared of the current voice.

DIR — This bit indicates the direction the sample is being scanned by the address ALU. A zero indicates the forward (incrementing) through memory, a one indicates the decrementing case. If the bidirectional looping mode has been selected the address ALU will automatically toggle this bit when the address reaches either the Loop Start or Loop End positions.

IRQE — This bit enables the Interrupt for the voice if IRQE=1.

BLE — Bidirectional looping enabled if BLE=1 and LPE=1.

LPE — Looping is enabled if LPE=1. Looping refers to restoring the address accumulator to the Loop Start position when the address accumulator exceeds the value in the Loop Stop register. If the LPE bit is a zero then the accumulator will stop when it reaches Loop Stop. The role of the Start and Stop positions is reversed if the DIR bit is a one. The state of BLE is ignored if LPE=0.

BS — This bank select bit is output on the BS pin at the same time as address for a memory cycle. It can be used to distinguish between 2 1Mword banks of ram in a 2Meg system. It can also be used as an external indication of the state of the voice counter.

STOP1 This bit is used by the processor to stop the address ALU from modifying any bits is a voice during its normal processing. For example, if this bit is set then the newly calculated address for the next sample will not be stored in to the address accumulator or the direction bit will not be changed. This feature allows the microprocessor to change the contents of either the control register or accumulator with concern.

STOP0 This bit performs the same function as the STOP1 bit. The difference is that this bit can be set by the address ALU. This bit is set when Looping is disabled and the accumulator reaches the Loop Stop position. Note that both STOP1 and STOP0 must equal zero for the voice to run.

The Frequency Control Register (FC) - 1

The Frequency Control Register is used to define the rate at which the address ALU will step through the sample memory. The register is a 15 bit word, left justified, that is divided into a 6 bit integer portion and a 9 bit fractional portion. At 10Mhz operation this yields an effective 2 cents resolution.

The Start Registers (STRT) - high=2, low=3

The Start Register, also called the Loop Start Register, is a 24 bit value divided into two register locations, namely registers 2 and 3. Register 2 contains the upper 13 bits of the Loop Start position while register 3 contains the lower 11 bit of the position. The upper 13 bits are right justified and lower 11 bits are left justified (See Register Map). The Loop Start position, as its name implies, is used to define where in the sample memory the accumulator will jump to when it reaches the Loop End position. Note that the Loop Start register has a 20 bit integer portion and a 4 bit fractional nibble. This fractional positioning capability allows much finer frequency resolution tuning when looping a waveform.

The End Registers (END) - high=4, low=5

The End Register, also called the Loop End Register, is partitioned the same way as the Start Register, a right justified 13 bit MSW and a left justified 11 bit LSW. It is used to mark the end of a loop in the sample memory. Note that the Start and End Registers reverse their roles if the Direction bit is a one. The End register contains the same integer and fractional partition as the Start register.

Filter Cutoff High (K2) - 6

The Filter Cutoff High Register is used to determine the 3dB point of poles three and four of the digital filter. It is a 12 bit register, left justified, using bits 15 through 4. The use of this register will be discussed in the explanation of the Digital Filter.

Filter Cutoff Low (K1) - 7

The Filter Cutoff Low Register is used to determine the 3dB point of poles one and two of the digital filter. It is a 12 bit register, left justified, using bits 15 through 4. The use of this register will be discussed in the explanation of the Digital Filter.

Left Volume (LVOL) - 8

The Left Volume Register is an 8 bit left justified register used to define the effective amplitude of the left channel of the sampled signal. It contains a 4 bit mantissa and a 4 bit exponent. The output of the filter is multiplied by a 5 bit value consisting a leading '1' followed by the 4 bit mantissa. The result of the multiplication is then shifted by the 4 bit exponent as shown below.

Right Volume (RVOL) - 9

This register is used to define the effective amplitude of the right channel of the sampled signal. Its' contains match those of LVOL. Together with LVOL it allows amplitude manipulation and stereo panning.

Accumulator (ACCH/ACCL) - high/low - A/B

The Accumulator is a 29 bit register divided into two parts, Accumulator High and Accumulator Low. The Accumulator high is 13 bits right justified ($ACCH_{12}$ thru $ACCH_0$) and the Accumulator low is a full 16 bit word ($ACCL_{15}$ thru $ACCL_0$). The Accumulator is comprised of an integer portion and a fractional portion. The integer part is 20 bits using $ACCH_{12}$-$ACCH_0$, $ACCL_{15}$-$ACCL_9$. This 20 bit value is the actual information used to fetch the sample data from memory. The 9 bit fractional part is needed to obtain proper frequency resolution and also for the interpolation calculation to be discussed in the Signal Processing section.

The Accumulator is also used as the waveform start position. This is not to be confused with the use of the Loop Start register. The initial Accumulator value is the beginning of the waveform while the Loop Start position defines the beginning of the sustain part of the waveform.

The Filter Storage Registers

Pages 32 through 63 are used to address six Filter Storage Registers in each voice. These registers are used as temporary storage location for the real time digital filters in each voice. Each digital filter requires six sixteen bit registers to complete is calculations. These six registers are addressable by the processor mainly for testing purposes and initialization, but there may be some yet to be determined audio benefits achieved by some real time processor intervention.

Note that when accessing these pages the global registers are still available.

Filter Pole 4(n-1) - Reg 1

A sixteen bit register containing the last output of final stage of the digital filter. This register is the actual data that is presented to the signal D to A converter.

Filter Pole 3(n-1) - Reg 2

A sixteen bit register containing the last output of the third stage of the digital filter. The output of this stage becomes the input to the fourth stage and the data pushed into Pole 3(n-2) on the next cycle.

Filter Pole 3(n-2) - Reg 3

A sixteen bit register which records the output of the third stage of the digital filter from the previous sample time. This information is needed to process the high pass filter mode of filter pole 4.

Filter Pole 2(n-1) - Reg 4

A sixteen bit register containing the last output of the second stage of the digital filter. The output of this stage becomes the input to the third stage and the data pushed into Pole 2(n-2) on the next cycle.

Filter Pole 2(n-2) - Reg 5

A sixteen bit register which records the output of the second stage of the digital filter from the previous sample time. This information is needed to process the high pass filter mode of filter pole 3.

Filter Pole 1(n-1) - Reg 6

A sixteen bit register containing the last output of the first stage of the digital filter. The output of this stage becomes the input to the the second stage.

2.3 THE CHANNEL REGISTERS

Pages 64 through 128 are used to address eight output channel registers mode register and the pot a/d conversion register. These registers are global to this address space and are accessed when the MSB of the page register is a 1.

Channel 0 Left/Right (CH0L/CH0R) - 0,1

These sixteen bit registers contain the accumulation of the result of the left and right volume multiplications. The registers are connected to serial port 0 and the PWM D/A output. They can be accessed only for testing these output sections. Therefore they can be written when the test bit of the SERMODE register is set, but can not be read.

Channel 1 Left/Right (CH1L/CH1R) - 2,3

These registers have the same function as CH0L/CH0R but they are not connected to PWM outputs. The registers are connected to serial port 1 and can be access for testing in the same way as CH0L/CH0R.

Channel 2 Left/Right (CH2L/CH2R) - 4,5

Same as CH1L/CH1R, but connected to serial port 2.

Channel 3 Left/Right (CH3L/CH3R) - 6,7

These registers serve the output function on serial port 3 as described above. Port can also be designated as a serial input by setting the A/D bit of the SERMODE register. This is to allow OTIS to accept digital information from an external A/D and hold the information for retrieval by the processor. For this reason these two registers are readable in any mode, but can only be written for testing as described above.

Serial Mode Register (SERMODE) - 8

This register contains the bits for configuring and testing the serial and PWM output ports. Following is a list of bits and there functions.

MSB[4:0] The channel registers are 16 bits with 5 guard bits to prevent overflow during accumulation. Since the bus interface is 16 bits, these 5 bits are prevented and are written to the 5 MSB's when a channel register is written. If these bits are not either all 0's or all 1's, then

overflow has occurred and the output will be saturated at either most positive or most negative depending on the state of MSB[4]. These bits are used to test the overflow detect logic of the channel registers.

SONY/BB — This bit designates that the serial input on port 3 during A/D mode follows either SONY or BURR-BROWN convention. SONY convention is that the first bit transferred occurs in the BCLK cycle immediately following assertion of WCLK. In BURR-BROWN format there is a 1 BCLK cycle delay after WCLK falls before the first bit of data is valid.

TEST — This bit turns of the signal accumulation function and allows write access to the channel registers. In this way the serial and PWM output sections can be isolated for testing.

A/D — This bit puts serial port 3 in input mode for accepting serial data from and external A/D. The serial data received is stored in CH3L/CH3R for access by the processor. This bit is set on chip reset to tristate the output to avoid contention.

Pot A/D register (PAR) - 9

This register contains the digital value resulting from the A/D conversion for tracking pots and wheels. The conversion is performed by comparing the input voltage on the POT pin to an internal reference ~2.8V. A internal pulldown on the POT pin discharged the pin. The pulldown is turned off allowing an external R-C to charge while the counter is clocked. When the voltage level on the input reaches the reference the value in the counter is loaded into this register for reading by the processor. The counter is clocked at 1.25Mhz, therefore, a conversion is done every 1.6ms

2.4 THE REGISTER MAP

PAGES 0 THROUGH 31

Reg	Symbol	Description	bits	Justification
0	CR	CONTROL REGISTER	12	[11:0]
1	FC	FREQUENCY CONTROL	15	[15:1]
2	STRT-H	LOOP START REG - HIGH	13	[12:0]
3	STRT-L	LOOP START REG - LOW	11	[15:5]
4	END-H	LOOP END REG - HIGH	13	[12:0]
5	END-L	LOOP END REG - LOW	11	[15:5]
6	K2	FILTER CUTOFF COEFFICIENT #2	12	[15:4]
7	K1	FILTER CUTOFF COEFFICIENT #1	12	[15:4]
8	LVOL	LEFT VOLUME	8	[15:12] EXP [11:8] MANT
9	RVOL	RIGHT VOLUME	8	[15:12] EXP [11:8] MANT
10	ACCH	ACCUMULATOR HIGH	13	[12:0]
11	ACCL	ACCUMULATOR LOW	16	[15:0]
13	ACT	NUMBER OF VOICES	5	[4:0]
14	IRQV	INTERRUPTING VOICE VECTOR	5	[4:0]
15	PAGE	PAGE SELECT REGISTER	7	[6:0]

PAGES 32 THROUGH 63

Reg	Symbol	Description	bits	Justification
1	O4(n-1)	FILTER 4 TEMP REGISTER	16	[15:0]
2	O3(n-1)	FILTER 3 TEMP REG #1	16	[15:0]
3	O3(n-2)	FILTER 3 TEMP REG #2	16	[15:0]
4	O2(n-1)	FILTER 2 TEMP REG #1	16	[15:0]
5	O2(n-2)	FILTER 2 TEMP REG #2	16	[15:0]
6	O1(n-1)	FILTER 1 TEMP REGISTER	16	[15:0]
13	ACT	NUMBER OF VOICES	5	[4:0]
14	IRQV	INTERRUPTING VOICE VECTOR	5	[4:0]
15	PAGE	PAGE SELECT REGISTER	6	[5:0]

PAGES 64 THROUGH 127

Reg	Symbol	Description	bits	Justification
0	CH0L	CHANNEL 0 LEFT	16	[15:0]
1	CH0R	CHANNEL 0 RIGHT	16	[15:0]
2	CH1L	CHANNEL 1 LEFT	16	[15:0]
3	CH1R	CHANNEL 1 RIGHT	16	[15:0]
4	CH2L	CHANNEL 2 LEFT	16	[15:0]
5	CH2R	CHANNEL 2 RIGHT	16	[15:0]
6	CH3L	CHANNEL 3 LEFT	16	[15:0]
7	CH3R	CHANNEL 3 RIGHT	16	[15:0]
8	SERMODE	SERIAL MODE	8	[15:11,2:0]
9	PAR	POT A/D REGISTER	10	[15:6]

2.5 DEFINITION OF SPECIFIC BITS IN THE MULTIPURPOSE REGISTERS

Reg	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
CR	1	1	1	1	LP4	LP3	CA1	CA0	IRQ	DIR	IRQE	BLE	LPE	BS	STP1	STP0
SERMODE	MSB4	MSB3	MSB2	MSB1	MSB0	1	1	1	1	1	1	1	1	SONY/BB	TEST	A/D

3 THE PIN DESCRIPTIONS

The following section describes the function of each of pins of the 5505.
The pins of the chip can be divided in to six functional categories, 1) clocks, 2) control, 3) address/data transfer, 4) serial port 5) playback outputs and 6) potentiometer a/d.

3.1 CLOCKS

CLKIN The CLKIN pin is the input clock for OTIS. The clock can be any frequency from 1 Mhz to 10Mhz. The clock input should be as close to 50-50 duty cycle as possible, since the chip times events on both input clock edges.

RAS The RAS pin is an output pin which generates a clock used to strobe the row address information into dynamic rams. This clock occurs whenever OTIS fetches data from memory (E clock low), or when the Memory Select (MSB) input line is low and the E clock is high. The RAS clock is high for one clock cycle and low for three clock cycles.

CAS The CAS pin is an output pin which generates a clock used to strobe the column address information into dynamic rams. This clock occurs whenever OTIS fetches information from memory (E clock low), or when the MSB input is low and the E clock is high. The CAS clock is high for two clock cycles and low for two clock cycles.

AMUX The AMUX pin is an output pin which generates a clock used to multiplex the row addresses and column addresses to the dynamic ram. The AMUX line is generated whenever RAS and CAS occurs. This clock is high for 1.5 clock cycles and low for 2.5 clock cycles, which means it occurs exactly between the RAS falling edge and the CAS falling edge.

E The E clock is an output used to indicate the current state of the OTIS chip. OTIS uses a shared bus structure, when the E signal is low OTIS accesses memory for sound generation and when E is high OTIS and the sound memory are available for access by the processor. The E clock is high for 4 clock cycles and low for four clock cycles. E is normally used to enable tristate buffers and gate the direction of data and address information to the dynamic memory. Note that even though the system shares memory the CSB, MSB and DTACK lines create as simply asynchronous bus communication environment.

3.2 CONTROL

R/W The R/W pin is an input that controls the direction of the data transfer between OTIS and the processor. When R/W is low the processor is writing data into OTIS. The R/W line is strobed at the rising edge of the E clock and if the CSB line is low OTIS will respond to the read/write request. The setup time for R/W is 0ns and the hold time after the rising edge of E is 100ns.

CSB The CSB (Chip Select) pin is an input used to select OTIS for a read or write operation. The CSB line is strobed at the rising edge of the E clock and if the CSB line is low OTIS will perform the operation requested by the R/W signal and generate a DTACK signal. The setup time for CSB is 0ns. and the hold time after the rising edge of E is 100ns.

MSB — The MSB (Memory Select) pin is an input used to assist in the processor access of shared dynamic memory. The MSB line is strobed at the rising edge of the E clock. The setup time is 0ns. and the hold time is 100ns. after the rising edge of the E clock. When the MSB line is low OTIS will generate RAS,CAS,AMUX, and DTACK during an E clock high cycle.

DTACKB — The DTACK pin is an open drain output used to synchronize the transfer of data between a 68000 microprocessor and OTIS or memory. The DTACK signal will go low during an E clock high cycle whenever the CSB or MSB line is low at the rising edge of the E clock. The DTACK line goes low two clock cycles after the rising edge of the E clock and will release at the falling edge of the E clock.

IRQ — The IRQ pin is an open drain output used to signal the processor that a special case has occurred that requires servicing. The line will go low when the interrupt is required by a particular voice. When the processor reads the Voice Vector register the line will then be released.

3.3 ADDRESS/DATA TRANSFER

A0-A3 — These four bidirectional lines are used for two purposes, determined by the state of the E clock. When E is high these pins are used as inputs, and allow the processor to access any of the data registers in OTIS. These address inputs must be valid 100ns. after the rising edge of the E clock and are latched at the falling edge of DTACK. When E is low these address lines are outputs used to address the external sound ram. These pins will output the voice address at the falling edge of the E clock. The address will remain valid until the falling edge of CAS at which time the pins will go to tristate.

A4/D0 - A19/D15 — These 16 lines are bidirectional and perform the data transfers from the processor or memory to OTIS. The function of this bus depends on the state of the E clock.

When the E clock is low these lines are first used to output the address for the sound memory access. The lines A0 through A3 together with A4 through A19 form the entire 20 bit address generated by OTIS. The addresses A4 through A19 will turn on 50ns. after E goes low and are valid 35ns. prior to the fall of RAS. The address will remain valid until the fall of CAS at which time the bus will go to the input mode to accept the data from the memory (D0 through D15).

When the E clock is high these 16 pins are used for data transfer only. If the CSB is low and the R/W line is high at the rising edge of the E clock then the chip will output the data from the register requested on pins A0 through A3. If both the CSB and the R/W lines low then the chip will accept the data from the bus and write it into the register specified by A0 through A3. The data is latched into the chip on the falling edge of the E clock.

BS — When the E clock is low this pin is driven based on the BS bit of the voice dependent control register. It can be used to select between 2 1Mword banks of sound memory. Since the state of this bit is voice dependent, it can also be used as an external indication as to the state of the voice counter.

3.4 SERIAL OUTPUT PORTS

SERBCLK — This is the bit clock for transfers on the serial port. It is a free running 2.5 Mhz clock.

SERWCLK — This is the word clock for transfers on the serial port. A low going transition on this clock signals the end of a 16 bit transfer. The 16 bits shifted previous to the transition should be latched as valid data.

SERLR — This is the left/right clock for transferring stereo information. It signifies left when in the high state and right when in the low state. Transitions on this clock occur with the first bit of a 16bit transfer.

SER0,1,2,3 — These are the serial data lines. Data is transferred on these lines in 2 word of 16bits each for stereo. Transfer begins with SERLR going high and the left MSB output on the data line. The each additional bit is clocked out on the falling edge of SERBCLK until the LSB of the 16 bit word is output. On the next falling edge of SERBCLK, the LSB of left is followed by the MSB for right, SERLR is negated and SERWCLK is driven low. SER3 is also capable of data input when the A/D bit of SERMODE is set.

3.5 PLAYBACK OUTPUTS

LHI,LHO
RHI,RLO — These outputs are left and write D/A outputs for the value in the channel 0 left and right and right registers. The use of these outputs will be discussed further later.

PWMZERO — This is a zero reference pulse to be used along with the above four signals for the playback scheme.

3.6 POTENTIOMETER A/D

POT — This pin is the input to a 10 bit A/D converter for tracking pots and wheels in the system. It's use is described previously in the description of the PAR register.

4 ALGORITHMS

The following section describes the data flow and algorithms used in OTIS. To adequately explain the the functions which eventually produce the the final output, the architecture will be presented in three sections, address generation, sample interpolation and digital filtering.

4.1 Address Generation

OTIS uses a technique called "Phase Accumulating Counters" to achieve pitch transposition of a previously sampled waveform. This technique uses an adder, an accumulator and a frequency control word. Each of these component pieces contains an integer and a fractional portion. At each voice time slot, the frequency control word is added to the accumulator and stored back to the accumulator. Consider, for example, that we wish to transpose a sinewave already in memory up one-half octave. This requires that we add to the accumulator the value 1.5 at each accumulation. This calculation can certainly be performed since all the structures have a fractional portion, but the sampled data does not contain a sample 35.5 for instance, only sample 35 or 36. In order to approximate sample 35.5 we must interpolate half way between the two data points contain in samples 35 and 36. Interpolation will be discussed in the next section, and is referred to here since the fractional aspect of the phase accumulating technique requires careful consideration when dealing with the looping.

In order to loop on a waveform the following algorithm is performed.

1. Fetch the Accumulator and put integer portion of accumulator on external address bus.
2. Add 1 to Accumulator and place on external address bus. This is used for interpolation. The incremented value is not retained.
3. Add Frequency Control Word to Accumulator
4. Subtract Loop End from Accumulator
5. If Loop End > Accumulator then add Frequency Control to Accumulator else add remainder of subtraction in Step 4 to Loop start.

As can be seen the remainder of the subtraction in step 4 is important to keep the phase of the waveform intact when looping and transposing. The counting algorithm presented here is used for all modes of looping except that the roles of the Loop Start and Loop End registers will be swapped depending on the direction of the count.

4.2 Interpolation

Once two successive samples have been fetched from the sound memory it is necessary to use linear interpolation to approximate a new sample. This approximation is done using by performing the following calculation.

SF = S1 + ACCfr * (S2 - S1), where

SF is the new sample,
S1 is first sample fetched,
S2 is the second sample fetched,
ACCfr is the 9 fractional bits of the Accumulator.

4.3 Digital Filtering

The new sample generated by linear interpolation is ready to be filtered. Each voice in OTIS is passed through four one pole filters. These digital filters each simulate a one pole Butterworth filter. As previously mentioned in the discussion of the filter configuration bits in register 9, filters one and two are fixed as low pass and filters three and four are selectable as either low pass or high pass. The table shown previously describes the four possible filter configurations and how the filter coefficients are applied.

The filter coefficients K1 and K2 are used to define the cutoff frequency of the filter. The following set of equations show the set of calculations performed on the sample data stream for each voice. The low pass filter is modeled by:

$$Y_n = K * (X_n - Y_{n-1}) + Y_{n-1}$$, where

Y_n is the new output,
K is cutoff coefficient,
X_n is the input,
Y_{n-1} is the previous output.

The high pass filter is modeled with:

$$Y_n = X_n - X_{n-1} + K * Y_{n-1}$$, where

Y_n is the new output,
K is cutoff coefficient,
X_n is the input,
X_{n-1} is the previous input.

The four filters are cascaded such that the output of the first is the input to the second and so on.

The coefficients K1 and K2 define the cutoff frequency of the filters. Given a desired attenuation (normally the -3dB point) the value for K can be determined from the following relationship for the low pass filter. Note that K is always a number less than 1.

$$K = \{1-\cos(W)-\sqrt{[\cos^2(w)+ (2/N^2)*[1-\cos(W)]-1]}\ \} /[1-(1/N^2)]$$, where

K is the cutoff coefficient,
$W = 2\pi f/F$, where f=frequency of interest and F is the sampling frequency,
N is the attenuation factor, .707 for -3dB.

A similar relationship can be developed for the high pass filter.

$$K = \{\cos(W)-\sqrt{[\cos^2(w)+ (2/N^2)*[1-\cos(W)]-1]}\}$$, where

K is the cutoff coefficient,
$W = 2\pi f/F$, where f=frequency of interest and F is the sampling frequency,
N is the attenuation factor, .707 for -3dB.

The most useful range of a high pass filter is generally below 4kHz. In order to maximize the resolution of the filter in that range an offset of .5 has been added to the K coefficient. This offset means the highest cutoff frequency achievable is approximately 8000Hz. for one high pass pole.

To determine the 12 bit digital value required for the K register perform the following calculation. For the low pass filter, multiply the value obtained from the previous equation by 4096. For the high pass filter subtract 0.5 and multiply by 8192.

Remember that the equations presented here are for one pole only, and the value for the

attenuation factor N must be scaled for the number of poles. For a one pole filter the 3dB point means N is equal to .707, a two pole filter requires each one pole filter to have N equal to .84, a three pole and N equals .89, etc.

4.4 Stereo Panning

The filter outputs go through a stereo pan calculation in which the signal is multiplied by left and right volume values to split into left and right signals. This allows panning with the same resolution as volume adjust. The volume values are contained in registers as a 4 bit mantissa and a 4 bit exponent. The computation is performed as follows:

1. The 16bit signal is multiplied by the value 1MMMM where M represents the bits of the mantissa.

2. The 16 MSB's of the result of step 1 are then shifted by the exponent as follows.

exponent	16 bit result															16 bit input = abcdefghijklmnop
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	a	a	a	a	a	a	a	a	a	a	a	a	a	a	a	b
2	a	a	a	a	a	a	a	a	a	a	a	a	a	a	b	c
3	a	a	a	a	a	a	a	a	a	a	a	a	a	b	c	d
4	a	a	a	a	a	a	a	a	a	a	a	a	b	c	d	e
5	a	a	a	a	a	a	a	a	a	a	a	b	c	d	e	f
6	a	a	a	a	a	a	a	a	a	a	b	c	d	e	f	g
7	a	a	a	a	a	a	a	a	a	b	c	d	e	f	g	h
8	a	a	a	a	a	a	a	a	b	c	d	e	f	g	h	i
9	a	a	a	a	a	a	a	b	c	d	e	f	g	h	i	j
A	a	a	a	a	a	a	b	c	d	e	f	g	h	i	j	k
B	a	a	a	a	a	b	c	d	e	f	g	h	i	j	k	l
C	a	a	a	a	b	c	d	e	f	g	h	i	j	k	l	m
D	a	a	a	b	c	d	e	f	g	h	i	j	k	l	m	n
E	a	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
F	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p

The result of the stereo pan calculation will be assigned to one of four channels based on the two voice dependent channel assign bits. These four channels are implemented as eight accumulating registers (left and right for each of four channels) and will sum signals during a complete sample cycle.

4.5 Serial Output and Playback

Once a cycle of the total number of voices has completed, the results of the channel accumulations are latched into shift registers and transmitted out through the serial port for used by external DSP's or D/A's. The accumulators are cleared to begin the next voice cycle. Since the bit clock for serial transmission is a 2.5MHz clock and each voice takes 1.6uS, A minimum of 8 voices must be used to insure enough time to transfer a full 32 bits of stereo information.

At the same time that the results are being output serially, the values in CH0L and CH0R are output on the playback outputs. The playback scheme is a pulse width modulated method. Each 16 bit register is separated into high and low bytes corresponding to the

LHI/LLO and RHI/RLO pins. At the start of a cycle all outputs are asserted, an internal 8 bit counter is clocked at a 10MHz rate and when the value of the counter matches one of the registers bytes, the output associated with that byte will be reset. The result is a pulse on the outputs whose width as measured in cycles of the 10MHz clock is the value in the register. Integrating these pulses and mixing the HI and LO with a ratio of 256:1 will produce an analog signal correspond to the 16 bit value for left and right. 256 cycles of the 10MHz clock are required to represent the maximum 8 bit value. This times corresponds to 16 voices at 1.6uS/voice and represents a 39KHz playback rate. More than 16 voices can be used but the playback rate will slow proportionally.

With more than 16 voices a negative offset would be introduced proportional to the number of voices above 16 (full scale). The PWMZERO output is supplied as a zero reference pulse with opposite polarity as the signal pulses. Because of the opposite polarity, greater than 16 voices will produce a positive offset on the reference pulse. The reference can therefore be mixed with the signal pulses to eliminate the offset problem.

4.6 INTERRUPT HANDLING

An interrupt can be caused by any active voice in OTIS. A voice will request interrupt servicing when the interrupt enable bit has been set and the accumulator has reached the loop end point (loop start if the direction bit is set). An interrupt will be issued by a voice regardless of the state of the loop mode bits when the accumulator reaches the loop end.

When an interrupt has been requested, the interrupt bit (bit 7 in the Control Register) is set, the voice number is latched into the Voice Interrupt Vector register and bit 7 of the Voice Vector register is cleared low. When the processor reads the Voice Vector register, bit 7 of the Voice Vector register is set high and when the voice which caused the interrupt is next processed, bit 7 of its Control Register is cleared.

If a voice has reached an interrupt condition and the Voice Vector is already contains information from another voice, that new requested will be stacked. This stacking occurs automatically since the interrupt bit in the Control Register of the voice will be set when the interrupt condition occurs. Eventually the processor reads the Voice Vector clearing the old interrupt vector information and the new vector will be placed in the register when the new voice is again processed. Note this ability allows the processor to force an interrupt from a voice simply by setting the interrupt enable bit and the interrupt bit of a particular voice.

5 ELECTRICAL SPECIFICATIONS

5.1 Maximum Ratings

Rating	Symbol	Value	Units
Supply Voltage	VDD	-3 to 7	V
Input Voltage	VIN	-3 to 7	V
Operating Temperature	TA	0 to 70	C
Storage Temperature	TSTG	-55 to 150	C

5.2 DC Electrical Characteristics

VDD = 5.0V ± 5%, VSS = 0V

Characteristic	Symbol	MIN	MAX	Units
Input High Voltage	VIH	2.0	VDD	V
Input Low Voltage	VIL	-0.5	0.8	V
Input Leakage Current VSS ≤ VIN ≤ VDD	IIN	-		uA
Hi-Z leakage @2.4V/0.5V	ITSI		-	
Output High Voltage IOH = (except DTACKB open collector)	VOH	2.4		V
Output Low Voltage IOL =	VOL	-	0.5	V
Input Capacitance	CIN	-		

5.3 AC Electrical Characteristics

Characteristic	Symbol	MIN	MAX	Units
Frequency of operation	f	5	10	Mhz
Clock Pulse Width	tCL,tCH	45	55	ns
Rise and Fall Times	tR,tF	5	5	
Clock low to E,RAS,CAS,AMUX	tCLA			
Address valid to RAS setup DOC read	tAVR			
Clock to DTACKB				
CSB,MSB,R/W setup to E				
Clock to Address valid				
Clock to Address tristate				
SERBCLK low to SERx				
SERBCLK low to SERWCLK				
SERBCLK low to SERLR				